INTEGRATED CIRCUIT FIFO MEMORY DEVICES THAT ARE DIVISIBLE INTO INDEPENDENT FIFO QUEUES, AND SYSTEMS AND METHODS FOR CONTROLLING SAME

Abstract of the Disclosure

Integrated circuit FIFO memory devices may be controlled using a register file, an indexer and a controller. The FIFO memory device includes a FIFO memory that is divisible into up to a predetermined number of independent FIFO queues. The register file includes the predetermined number of words. A respective word is configured to store one or more parameters for a respective one of the FIFO queues. The indexer is configured to index into the register file, to access a respective word that corresponds to a respective FIFO queue that is accessed. The controller is responsive to the respective word that is accessed, and is configured to control access to the respective FIFO queue based upon at least one of the one or more parameters that is stored in the respective word. Thus, as the number of FIFO queues expands, the number of words in the register file may need to expand, but the controller and/or indexer need not change substantially. The register file may include multiple register subfiles, and the controller may include multiple controller subblocks.